Designing a Dynamic Ramp With an Invariant Inductor in Current-Mode Control for an On-Chip Buck Converter

Wen-Wei Chen, *Student Member, IEEE*, Jiann-Fuh Chen, *Member, IEEE*, Tsorng-Juu Liang, *Senior Member, IEEE*, Lu-Chi Wei, and Wei-Yuan Ting

***Abstract*—Designing a dynamic ramp with an invariant inductor in current-mode control for an on-chip Buck converter is proposed in this paper. This configuration maintains system stability under different input/output voltages without changing the inductor and compensation circuit. The dynamic ramp can be adjusted according to the variation in the output voltage or the voltage droop between the input voltage and the output voltage to maintain bandwidth and phase margin using the invariant inductor and compensation circuit. Finally, 14-V input voltage, 12-V output voltage, and 24-W output power with the dynamic ramp sampling the output voltage is implemented using MathCAD predictions, SIMPLIS simulation results, and experimental results to verify its viability and superiority.**

***Index Terms*—Current-mode control, dynamic ramp, invariant inductor.**

I. Introduction

In a dc–dc Buck converter, the current-mode control is widely used to achieve better transient response [1]–[10]. The current-mode control contains two feedback signals. The output voltage is fed into an error amplifier to generate a control signal. The inductor current is sampled and compared with the control signal to control the peak inductor current, thus regulating the output voltage to the specified level. The inductor current feedback causes the control to have a better transient response. However, it also produces a subharmonic issue when the duty cycle is larger than 50%.

A ramp compensation signal is always added into the control loop to prevent subharmonic [1]–[5], [11]–[13], as shown in Fig. 1. The ramp compensation is designed according to the inductor current ripple determined by the input voltage, output voltage, and inductance. A general-control integrated circuit (IC) often imbeds a fixed ramp into the control loop. However, this kind of chip is usually designed for a wide input and output range, thus resulting in a varied inductor current ripple in the entire operation range. Meeting the fixed ramp compensation requires that the inductance is changed to maintain the same current ripple. Thus, the compensation circuit should also be modified to keep system bandwidth, gain margin, and phase margin. This modification is not convenient for the user and designer.

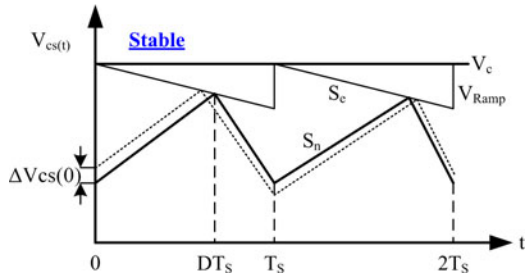

Fig. 1. Ramp compensation to prevent subharmonic.

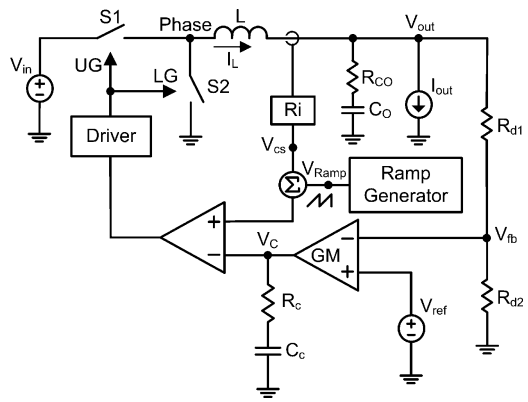

Fig. 2. Fixed ramp in current-mode control for a Buck converter.

Fig. 2 shows the fixed ramp in current-mode control for a Buck converter. S1 and S2 are the switches, UG is upper control signal to drive the switch S1, LG is lower control signal to drive the switch S2, L is the output inductor, and $R_{\rm CO}$ is the equivalent series resistance (ESR) of the output capacitor C_O. The current source $I_{\rm out}$ is the output load, and R_{d1} and R_{d2} are the feedback resistors to determine the output voltage. The feedback voltage

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TABLE I
OPERATION CONDITIONS IN CURRENT-MODE CONTROL FOR A BUCK CONVERTER

V_{in} (V)	21 V	F_S (kHz)	400 kHz	L (μH)	15 μH
V_{out} (V)	12 V	R_{d1} (kΩ)	140 kΩ	C_O (μF)	22 μF
I_{out} (A)	2 A	R_{d2} (kΩ)	10 kΩ	R_{CO} (mΩ)	3 mΩ
V_{ref} (V)	0.8 V	R_i (A/V)	0.4		

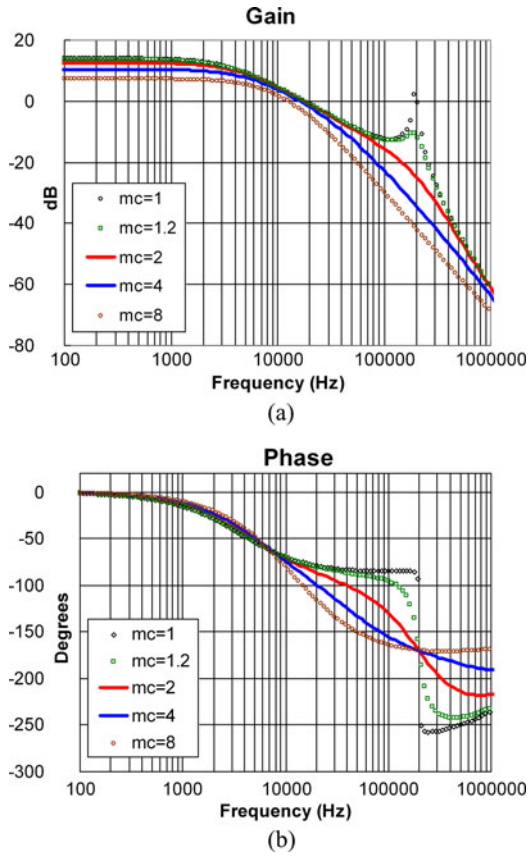

Fig. 3. Open-loop control-to-output Bode plot with different *mc*. (a) Gain. (b) Phase.

$V_{\rm fb}$ and the reference voltage $V_{\rm ref}$ are built inside the IC. R_C and C_C are the compensator parameters to adjust the system loop stability.

Table I lists the operation conditions in current-mode control for a Buck converter, where *mc* is expressed by (1) and (2). S_e is a slope of the ramp compensation and S_n is the inductor on-time slope and $D' = 1 - D$. Based on Table I, the open-loop control-to-output Bode plot with different *mc* values is plotted in Fig. 3

$$mc = 1 + \frac{S_e}{S_n} \tag{1}$$

$$S_n = \frac{V_{\rm in} - V_{\rm out}}{L} \cdot R_i. \tag{2}$$

In Fig. 3 [1]–[5], the gain curves of *mc* values 1 and 1.2 present no ramp compensation and small ramp compensation, respectively. Both of these values have a double pole that can cause a high Q at half of the switching frequency. The double pole causes a sharp phase drop of 180°, thus resulting in subharmonic and an unstable system. However, if the ramp compensation is large, as presented by the gain curve of *mc* = 8, then the control loop has formed as a voltage-mode control, given that the ramp compensation is much larger than the inductor current. Therefore, a proper *mc* value between 2 and 4 should be designed to prevent subharmonic and to ensure the stability of the system.

TABLE II
RECOMMENDED COMPONENT SELECTION

Conditions	V_{in}=3.3V~21V, F_S=400kHz, I_{out}=2A			
Fixed Ramp	V_{Ramp}=306 mV (IC Internal Parameter)			
V_{out} (V)	R_c (kΩ)	C_c (nF)	L (μH)	C_O (μF)
12	40	2.2	33	22
5	20	2.2	22	22
3.3	10	1.5	15	22
1.8	6	1.5	10	22

TABLE III
SAME INDUCTANCE AND CAPACITANCE UNDER DIFFERENT OUTPUT VOLTAGES

Conditions	V_{in}=3.3V~21V, F_S=400kHz, I_{out}=2A			
Fixed Ramp	V_{Ramp}=306 mV (IC Internal Parameter)			
V_{out} (V)	R_c (kΩ)	C_c (nF)	L (μH)	C_O (μF)
12	10	1.5	15	22
5	10	1.5	15	22
3.3	10	1.5	15	22
1.8	10	1.5	15	22

II. CONVENTIONAL RAMP COMPENSATION IN CURRENT-MODE CONTROL FOR A BUCK CONVERTER

Most wide-input range Buck converters provide a recommended component selection table to maintain parameter *mc* in a proper range, as listed in Table II [14], [15]. In order to meet the fixed ramp compensation requires that the inductance is changed to maintain the same current ripple when the user determines to apply different output voltages. Thus, the compensation circuit should also be modified to keep the system stability. This modification is not convenient for the user and designer. Therefore, this paper proposes a novel control scheme to solve this issue.

Table III lists the same inductance and capacitance under different output voltages in current-mode control for a Buck converter. Based on the conditions listed in Table III, Bode plot is constructed to illustrate system stability, as shown in Fig. 4. The operation of the input voltage is 14 V for the worst case scenario (high duty cycle). Inductance and capacitance are also selected at 15 μH and 22 μF, respectively, under different output voltages. Fig. 4 shows that the gain curve of the output voltage of 12 V contains a double pole which can result in a high Q at half of the switching frequency. The double pole causes a sharp phase drop of 180°, which means that the system suffers from a subharmonic issue at the output voltage of 12 V.

III. DYNAMIC RAMP COMPENSATION IN CURRENT-MODE CONTROL FOR A BUCK CONVERTER

Fig. 5 shows the dynamic ramp sampling the output voltage in current-mode control for a Buck converter. The ramp generator

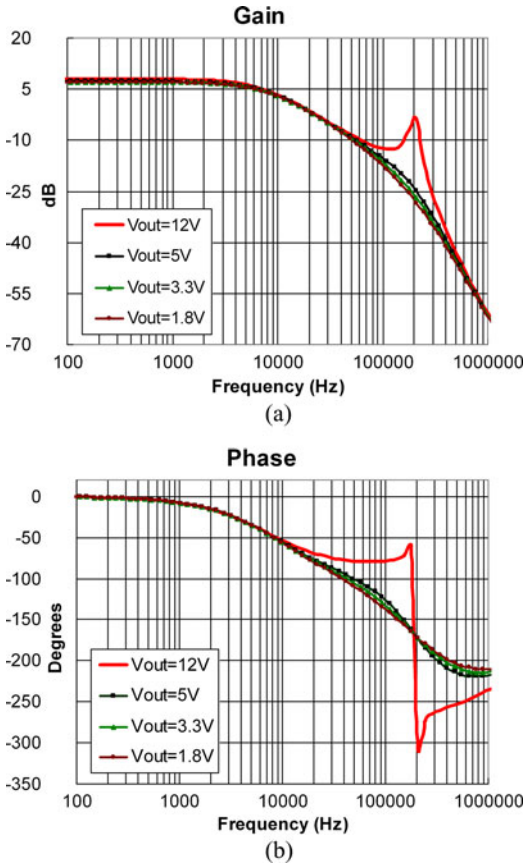

Fig. 4. Open-loop control-to-output Bode plot with different output voltages at the input voltage 14 V. (a) Gain. (b) Phase.

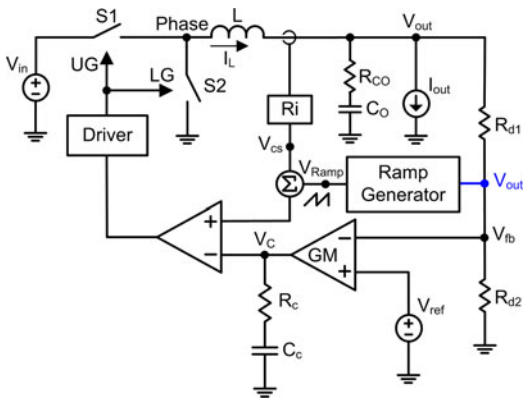

Fig. 5. Dynamic ramp sampling the output voltage in current-mode control for a Buck converter.

can only sample the output voltage or the output voltage and input voltage, to implement a dynamic ramp. The output voltage is changed large, and the dynamic ramp is increased to prevent the system suffering from a subharmonic issue.

Fig. 6 shows that the dynamic ramp is dependent on the output voltage. The duty cycle D_1 is small than 50% as shown in Fig. 6(a) and the duty cycle D_2 larger than 50% as shown in Fig. 6(b). Duty cycle D_1 is smaller than the duty cycle D_2 and the slope of S_{n1} is steeper than that of S_{n2}. The ramp generator yields the new ramp compensation V_{Ramp2}, which has the slope

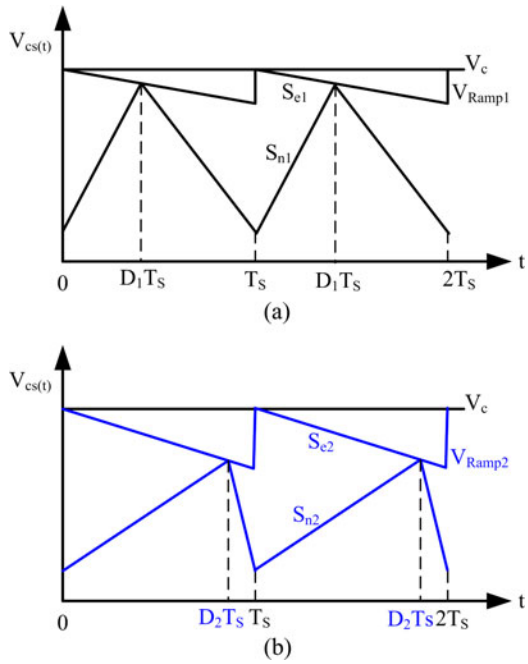

Fig. 6. Dynamic ramp depended on the output voltage. (a) Duty cycle small than 50% (b) Duty cycle larger than 50%.

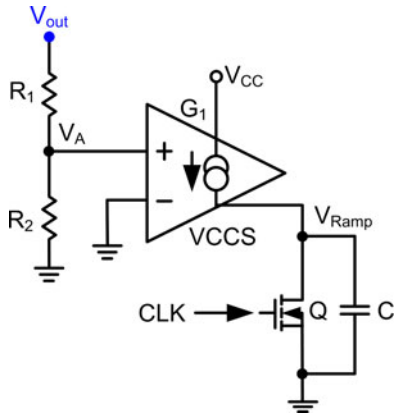

Fig. 7. Implementation of a dynamic ramp generator sampling the output voltage.

of S_{e2} steeper than that of S_{e1}. Thus, ramp compensation is not fixed but dynamic.

Fig. 7 shows the implementation of the dynamic ramp generator sampling the output voltage. The voltage V_A depends on the output voltage. The voltage V_A is also an input signal for the voltage-controlled current source (VCCS). The output signal of VCCS charges capacitor C to generate the dynamic ramp V_{Ramp}, which can be calculated by

$$V_{\mathrm{Ramp}} = \frac{G_1 (V_{\mathrm{out}} \times \frac{R_2}{R_1 + R_2})}{C * Ts}. \tag{3}$$

Fig. 8 shows the block diagram of the dynamic ramp sampling the output voltage in the current-mode control for a Buck converter. In the block diagram, the switches of the power stage are replaced with a three-terminal switching model [1]–[4], [10], [16]–[25], in which the ideal transformer plays the role of the

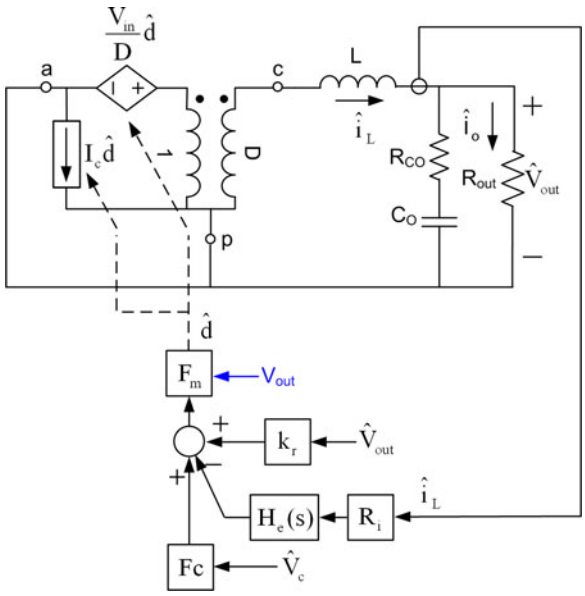

Fig. 8. Block diagram of the dynamic ramp sampling the output voltage in current-mode control for a Buck converter.

average duty cycle, and the two dependent sources model the perturbation of the duty cycle. According to the block diagram, transfer functions can be derived to analyze system stability. The transfer functions of control-to-output are shown in (4) to (9). *mc* should be designed at an optimum proportion between S_n and S_e to obtain the suitable signal for S_e

$$\frac{\hat{V}_{\text{out}}}{\hat{V}_c} \cong \frac{R_{\text{out}}}{R_i} \cdot \frac{1}{1+\frac{R_{\text{out}}}{L\cdot F_S}\left[\left(1+\frac{S_e}{S_n}\right)\cdot D' - 0.5\right]} \cdot Fp(s)\cdot Fh(s) \tag{4}$$

$$Fp(s) = \frac{1+s\cdot C_O\cdot R_{CO}}{1+\frac{s}{\omega_P}} \tag{5}$$

$$Fh(s) = \frac{1}{1+\frac{s}{\omega_n\cdot Q_P}+\frac{s^2}{\omega_n^2}} \tag{6}$$

$$\omega_P = \frac{1}{C_O\cdot R_{\text{out}}} + \frac{1}{C_O\cdot L\cdot F_S}\cdot\left[\left(1+\frac{S_e}{S_n}\right)\cdot D' - 0.5\right] \tag{7}$$

$$Q_P = \frac{1}{\pi\cdot\left[\left(1+\frac{S_e}{S_n}\right)\cdot D' - 0.5\right]} \tag{8}$$

$$\omega_n = \pi\cdot Fs. \tag{9}$$

Based on the conditions listed in Table III for optimized *mc* values, inductance and capacitance are selected at 15 μH and 22 μF, respectively, at the input voltage of 14 V and the output voltage of 12 V, under different *mc* values of 3, 6, and 9, as shown in Fig. 9.

The gain curve of $mc = 3$ contains a high Q at half of the switching frequency caused by a double pole. The gain curve of $mc = 9$ has a voltage mode behavior similar to having no current loop function. Finally, the gain curve of $mc = 6$ is optimum for

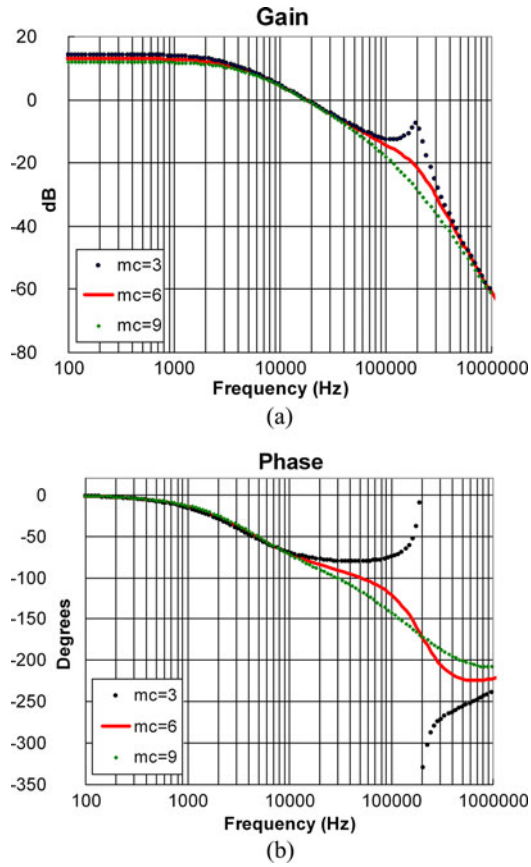

Fig. 9. Open-loop control-to-output Bode plot with different *mc* at the input voltage 14 V and the output voltage 12 V. (a) Gain. (b) Phase.

designing the proportion between S_n and S_e. This system is stable to operate at a high duty cycle and also uses the invariant inductor to prevent subharmonic. The dynamic ramp is designed based on the gain curve of $mc = 6$. Ramp generator parameters G_1, R_1, R_2, and C are calculated by (10). Assuming that R_1 is 100 kΩ, R_2 is 10 kΩ, and C is 10 pF, then gain G_1 of VCCS is 2.6667 μ

$$\frac{G_1(V_{\text{out}}\times\frac{R_2}{R_1+R_2})}{C} \geq 5\times\frac{(V_{\text{in}}-V_{\text{out}})}{L}\cdot R_i. \tag{10}$$

Fig. 10 shows the open-loop control-to-output Bode plot of the dynamic ramp sampling the output voltage at the input voltage of 14 V. The open-loop control-to-output for Buck converter using the dynamic ramp exhibits the same Bode plot for the gain and phase under different output voltages. This system does not only use the invariant inductor, but also designs the same compensation circuit to meet different applications when the output voltage is changed. Therefore, the proposed dynamic ramp sampling the output voltage is very simple and easy to implement.

The ramp generator can also sample the output voltage and the input voltage to implement the dynamic ramp. The voltage droop between the input voltage and the output voltage is changed from large to small, and the dynamic ramp is increased to prevent the system suffering from a subharmonic issue. Fig. 11 shows the implementation of the dynamic ramp generator with sampling the output voltage and input voltage.

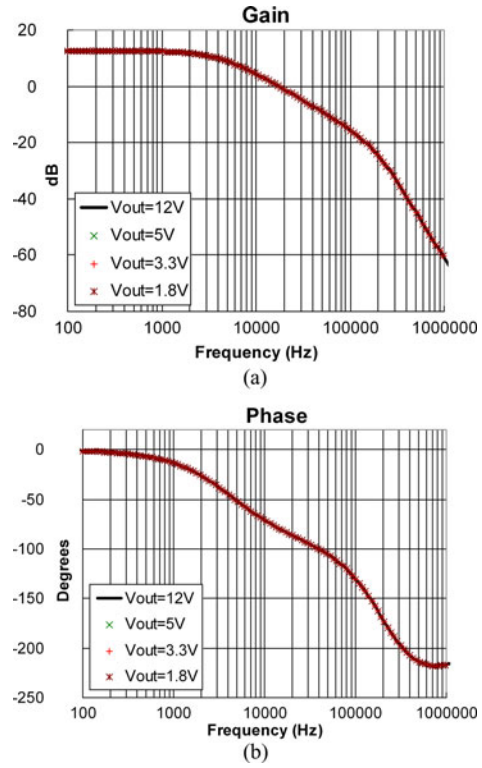

Fig. 10. Open-loop control-to-output Bode plot with dynamic ramp sampling the output voltage at the input voltage 14 V. (a) Gain. (b) Phase.

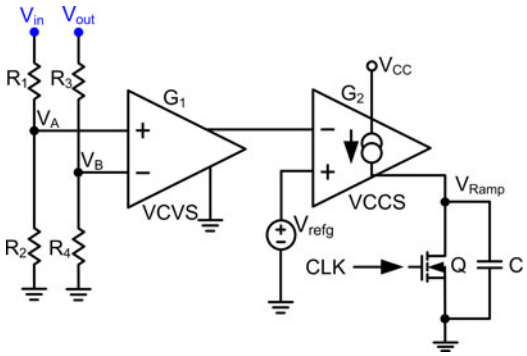

Fig. 11. Implementation of the dynamic ramp generator with sampling the output voltage and the input voltage.

The voltage V_A depends on the input voltage. The voltage V_A is also an input signal for a voltage-controlled voltage source (VCVS). The voltage V_B depends on the output voltage. This voltage is the other input signal for a VCVS. G_1 is the gain of VCVS. G_1 is also a unity gain. The output signal of VCVS is an input signal for VCCS. G_2 is the gain of VCCS. The output signal of VCCS charges capacitor C to generate the dynamic ramp V_{Ramp}, which can be calculated by (11). Otherwise, the voltage signal V_{refg} should be designed to be larger than the voltage droop between V_A and V_B

$$V_{\mathrm{Ramp}} = \frac{G_2\left[V_{\mathrm{refg}} - \left(V_{\mathrm{in}} \times \frac{R_2}{R_1+R_2} - V_{\mathrm{out}} \times \frac{R_4}{R_3+R_4}\right)\right]}{C * Ts}. \tag{11}$$

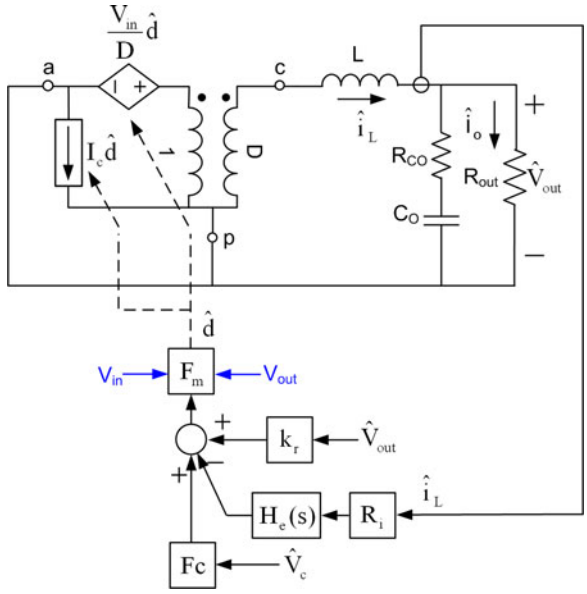

Fig. 12. Block diagram of the dynamic ramp with sampling the output voltage and the input voltage in current-mode control for the Buck converter.

Fig. 12 shows the block diagram of the dynamic ramp with sampling the output voltage and input voltage in the current-mode control for a Buck converter. Finally, the gain curve of $mc = 6$ is also optimum for designing the proportion between S_n and S_e as shown in Fig. 9. This system is stable to operate at a high duty cycle and also uses the invariant inductor to prevent subharmonic. Ramp generator parameters $G_2, R_1, R_2, R_3, R_4, V_{\mathrm{refg}}$, and C are calculated by (12).

Assuming that R_1 and R_3 are both 100 kΩ, R_2 and R_4 are both 10 kΩ, and C is equal to 28 pF; then, V_{refg} is equal to 1.5 V, and gain G_2 of VCCS is 3.2 μ.

Fig. 13 shows the open-loop control-to-output Bode plot of the dynamic ramp sampling the output voltage and the input voltage at the input voltage of 14 V. According to the same Bode plot, this system does not only use the invariant inductor, but also designs the same compensation circuit to meet different applications when the output voltage is changed. Therefore, the proposed dynamic ramp sampling the output voltage and the input voltage is very simple and easy to implement.

IV. Experimental Verification

MathCAD predictions, SIMPLIS simulation results, and experimental verifications were conducted to determine the feasibility and performance of the proposed dynamic ramp with the invariant inductor in current-mode control for an on-chip Buck converter.

The specifications are as follows:

1) input dc voltage range V_{in}: 5 ∼ 21 V;
2) output dc voltage range V_{out}: 1.222 ∼ 16 V;
3) maximum output load I_{out}: 2 A;
4) switching frequency F_S: 400 kHz;
5) feedback resistors R_{d1} and R_{d2}: 115 kΩ and 13 kΩ;
6) main inductor L: IHLP4040DZER1R0MA1 (15 μH);
7) output capacitors C_O: 22 μF/ 25 V∗1 ($\mathrm{R_{CO}}$: 3 mΩ);

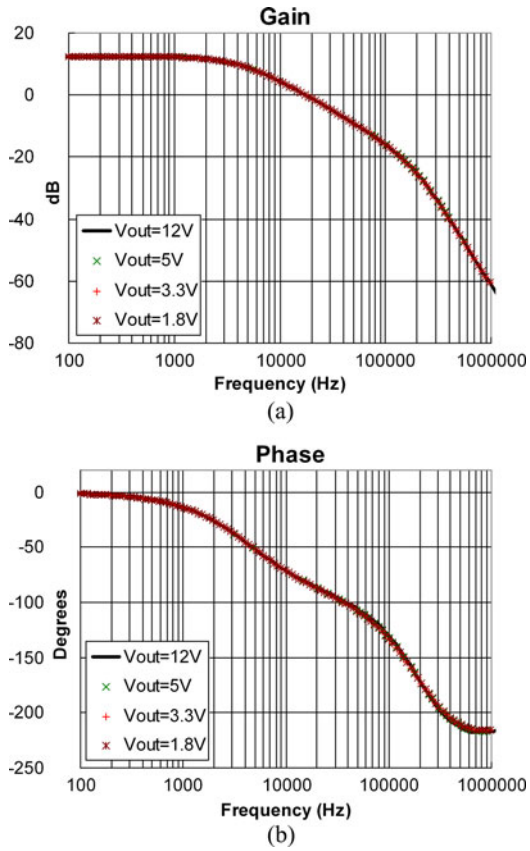

Fig. 13. Open-loop control-to-output Bode plot of the dynamic ramp sampling the output voltage and the input voltage at the input voltage 14 V. (a) Gain. (b) Phase.

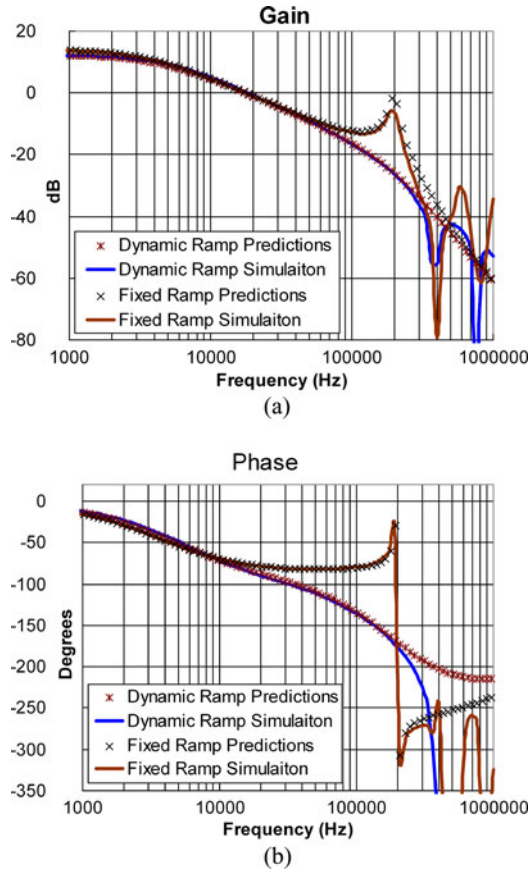

Fig. 14. Comparison of MathCAD predictions and SIMPLIS simulation results for open-loop control-to-output Bode plot using the dynamic ramp and the fixed ramp. (a) Gain. (b) Phase.

8) reference voltage $V_{\rm ref}$: 1.222 V;
9) dynamic ramp circuit (see Fig. 7): $G_1 = 2.6667\ \mu$V/A; $C_1 = 10$ pF; $R_1 = 100$ kΩ; $R_2 = 10$ kΩ;
10) fixed ramp circuit: $V_{\rm Ramp} = 0.306$ V;
11) compensator circuit: $R_c = 10$ kΩ; $C_c = 1.5$ nF.

Fig. 14 compares MathCAD predictions and SIMPLIS simulation results for the open-loop control-to-output Bode plot using the dynamic ramp and the fixed ramp. MathCAD is used for predicting results in calculating equations for the dynamic ramp and the fixed ramp. SIMPLIS is used to simulate results for the dynamic ramp and the fixed ramp. MathCAD prediction results are very similar to SIMPLIS simulation results. The fixed ramp has a high Q at half of the switching frequency caused by a double pole. The double pole causes a sharp phase drop of 180° at 200 kHz, which is also located at half of the switching frequency, thus resulting in a subharmonic issue and an unstable system.

Fig. 15 compares MathCAD predictions and SIMPLIS simulation results for the closed-loop loop gain Bode plot using the dynamic ramp and the fixed ramp. In Fig. 15, MathCAD prediction results are very similar to SIMPLIS simulation results. Both MathCAD prediction and SIMPLIS simulation result verifications confirm that the proposed dynamic ramp with the invariant inductor in current-mode control for the Buck converter can significantly prevent subharmonic. The bandwidths of the fixed ramp for the SIMPLIS simulation results and MathCAD predictions are both 20 kHz, whereas the bandwidths of the dynamic ramp for SIMPLIS simulation results and MathCAD predictions are very close to each other. The phase margin of the dynamic ramp is very close to the fixed ramp.

Fig. 16 shows the chip layout of the control IC. The control IC was used by TSMC 0.6 μm process and Rds_on of the main switch is 180 mΩ. The Power MosFET, driver circuit, control circuit, and current sensor occupy the marked area with a die size of 1250 μm $\times$ 960 μm.

Fig. 17 shows the output voltage and the UG signal using the fixed ramp at the input voltage of 14 V, the output voltage of 12 V, and the output load of 2 A. Experimental results are measured at the output voltage and the UG signal for the fixed ramp. The experimental result of the output voltage ripple for the fixed ramp is equal to 27.2 mV. The UG signal for the fixed ramp exhibits subharmonic; thus, the width of the UG signal is not the same.

Fig. 18 shows the output voltage and the UG signal using the dynamic ramp at the input voltage of 14 V, the output voltage of 12 V, and the output load of 2 A. Experimental results are measured at the output voltage and the UG signal for the dynamic ramp. The experimental result of the output voltage ripple for the dynamic ramp is equal to 6.8 mV. The UG signal does not exhibit subharmonic and the width of the UG signal is the same.

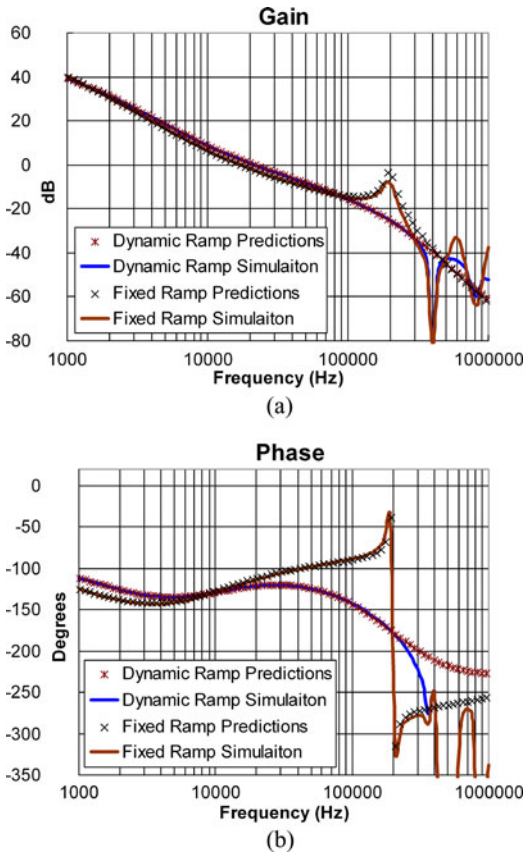

Fig. 15. Comparison of MathCAD predictions and SIMPLIS simulation results for closed-loop loop gain Bode plot using the dynamic ramp and the fixed ramp. (a) Gain. (b) Phase.

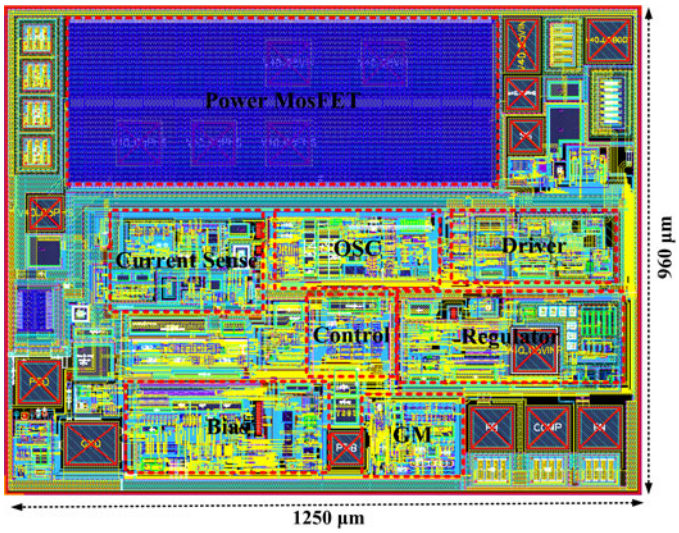

Fig. 16. Chip layout of the control IC.

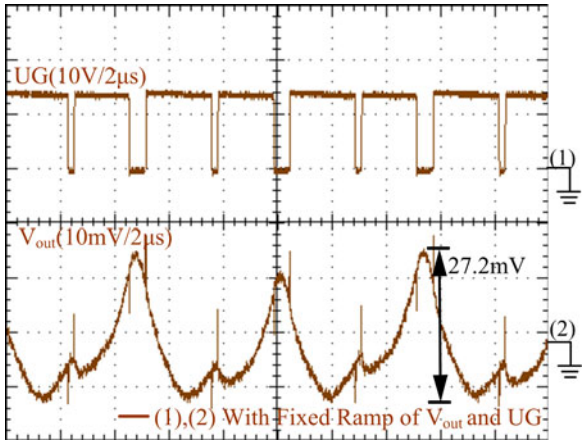

Fig. 17. Output voltage and the UG signal using the fixed ramp at the input voltage 14 V and the output voltage 12 V.

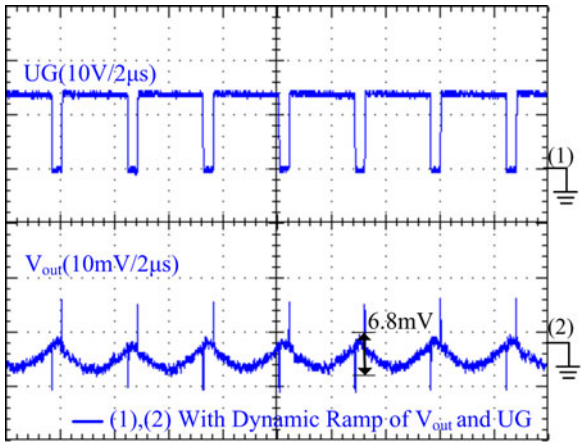

Fig. 18. Output voltage and the UG signal using the dynamic ramp at the input voltage 14 V and the output voltage 12 V.

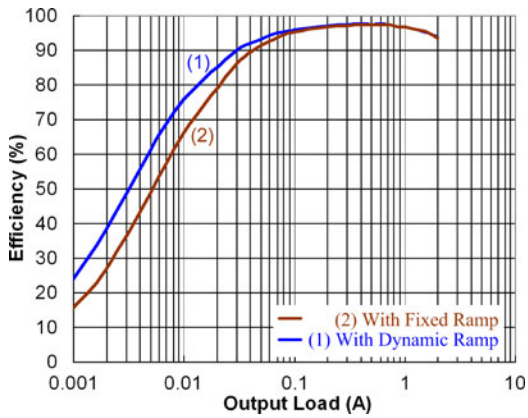

Fig. 19. Comparison of the experimental results for efficiency using the dynamic ramp and the fixed ramp at the input voltage 14 V and the output voltage 12 V.

Fig. 19 compares of the experimental results for efficiency using the dynamic ramp and the fixed ramp at the input voltage 14 V and the output voltage 12 V in current-mode control for the Buck converter. The current-mode control using the dynamic ramp for the Buck converter has higher efficiency than the fixed ramp during the output load from 1 mA to 0.1 A, because the fixed ramp has the subharmonic to cause high switching loss. When the output load has increased, the efficiency of that with the fixed ramp is very close to that with the dynamic ramp, because the conduction loss is a major factor that affects the efficiency in this condition.

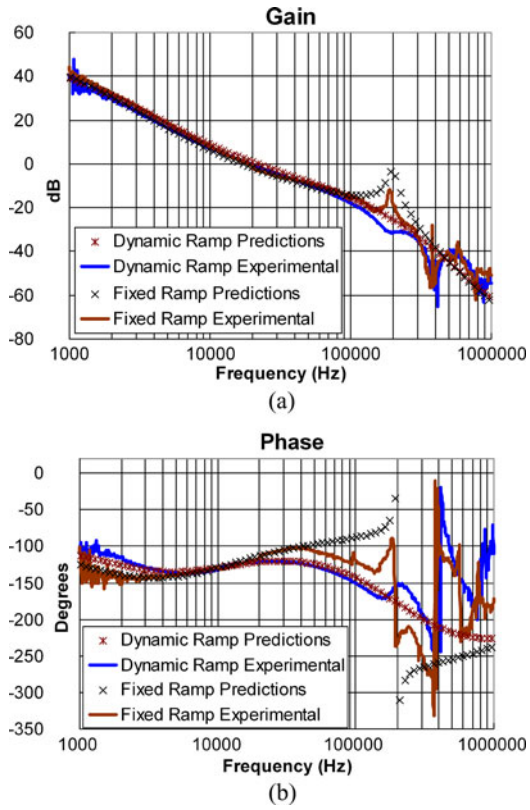

Fig. 20. Comparison of MathCAD predictions and experimental results for closed-loop loop gain Bode plot using the dynamic ramp and the fixed ramp. (a) Gain. (b) Phase.

Fig. 20 compares MathCAD predictions and experimental results for the closed-loop loop gain Bode plot using the dynamic ramp and the fixed ramp. MathCAD prediction results are very similar to experimental results. Both MathCAD prediction and experimental result verification confirm that the proposed dynamic ramp with the invariant inductor in current-mode control for an on-chip Buck converter can significantly prevent subharmonic. The gain curve of the fixed ramp contains a high Q at 200 kHz, which is also located at half of the switching frequency caused by a double pole.

The dynamic ramp and fixed ramp both uses the same compensation parameters to obtain MathCAD predictions and experimental results. The bandwidths of the fixed ramp for the experimental results and MathCAD predictions are both 20 kHz, whereas the bandwidths of the dynamic ramp for the experimental results and MathCAD predictions are very close to each other. The phase margin of the dynamic ramp is very close to the fixed ramp for both the experimental results and MathCAD predictions.

V. Conclusion

Experimental results, SIMPLIS simulation results, and MathCAD predictions confirm that the proposed dynamic ramp with the invariant inductor in current-mode control for an on-chip Buck converter does not only maintain system stability under different input/output voltages without changing the inductor and compensation circuit, but also significantly prevents subharmonic. Moreover, the proposed dynamic ramp has a very simple structure and easy-to-implement design. This system is available and useful as a current-mode control for the Buck converter.

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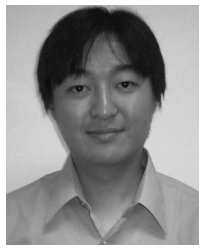

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